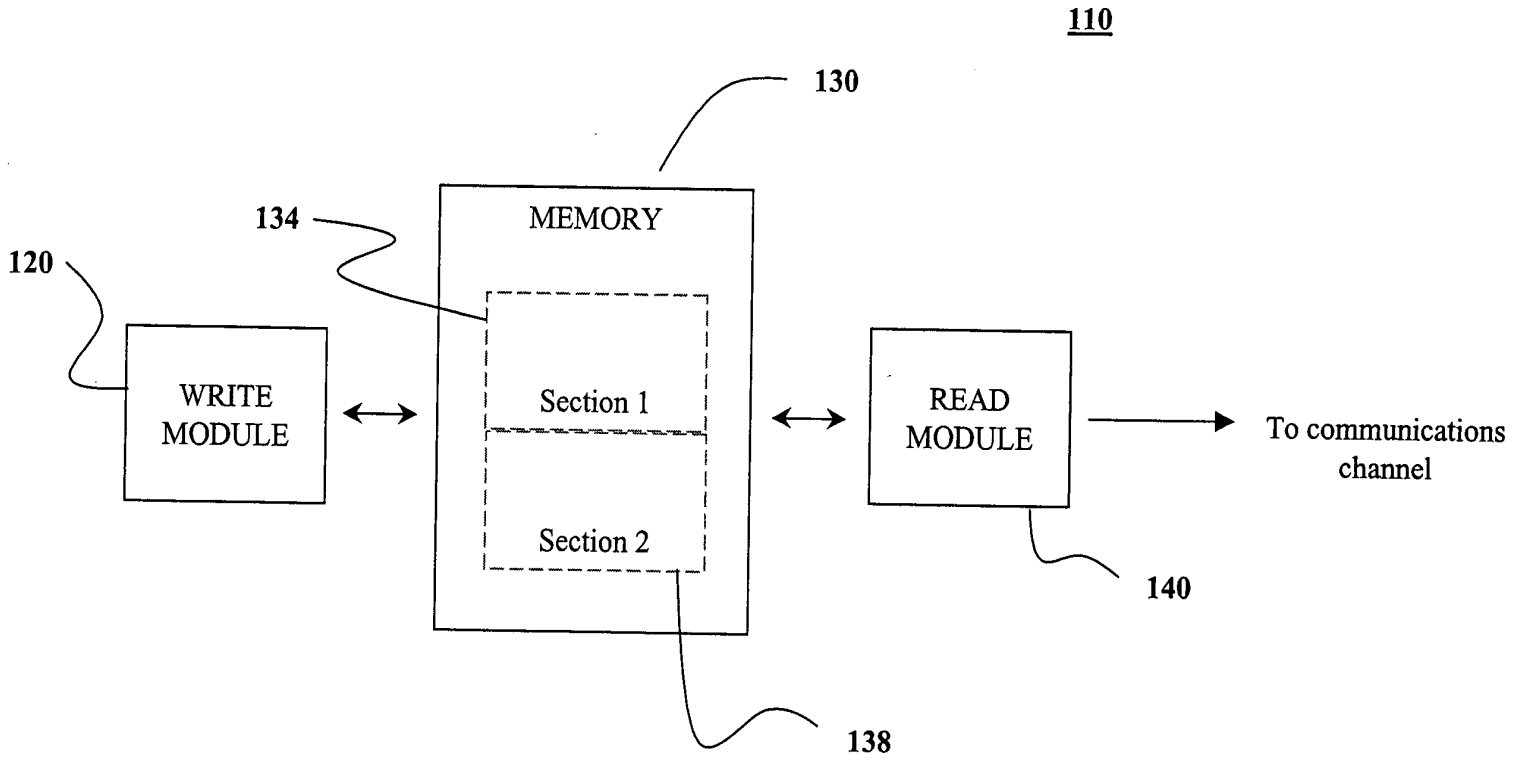

FIG. 1
RELATED ART

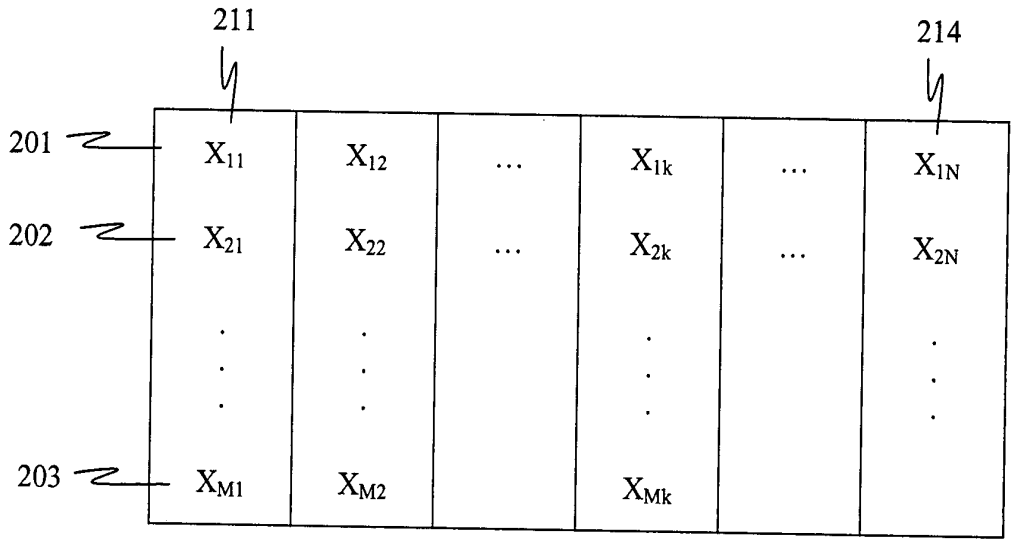

FIG. 2
RELATED ART

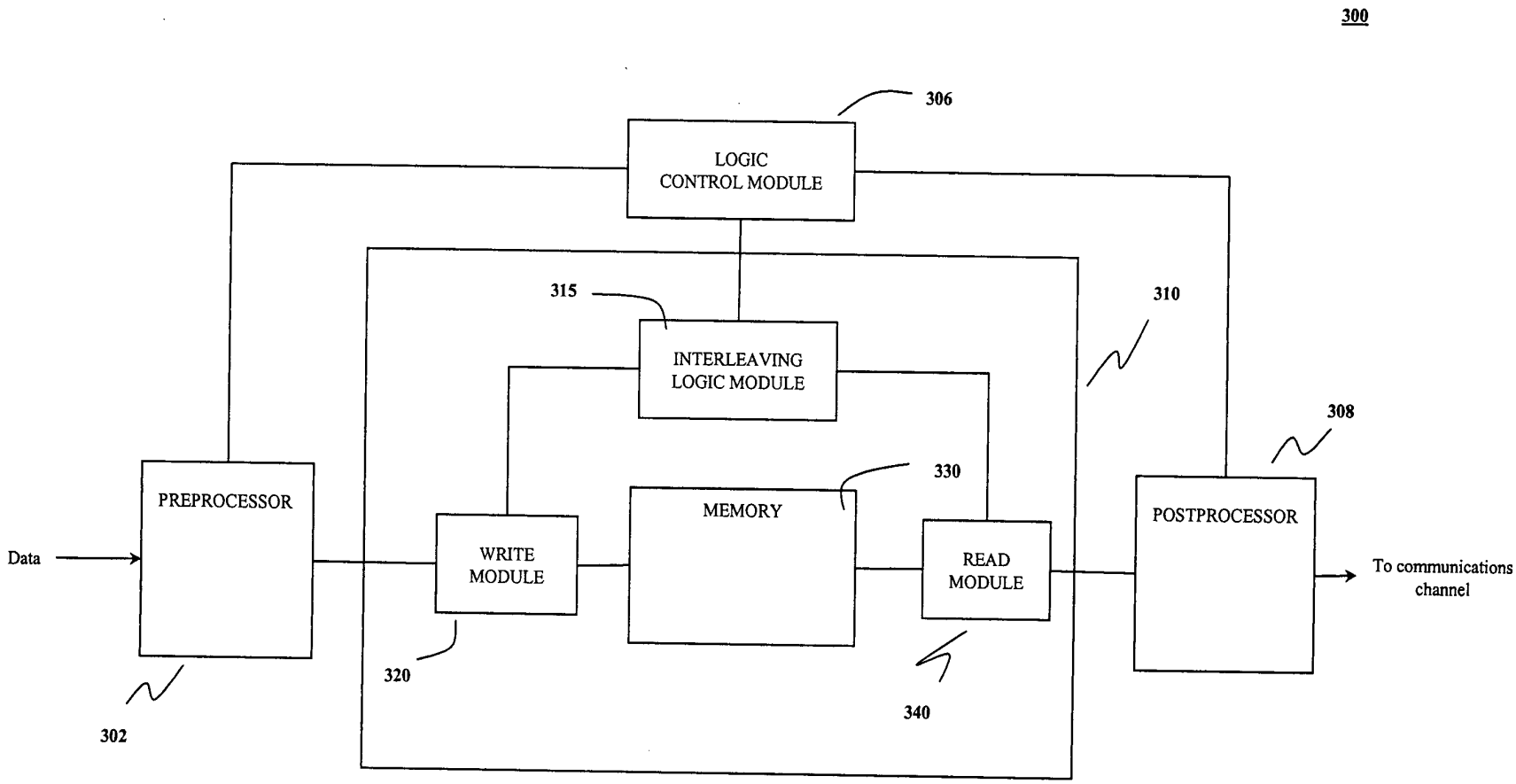
300
306
LOGIC
CONTROL MODULE
315
310
INTERLEAVING
LOGIC MODULE
308
330
PREPROCESSOR
MEMORY
POSTPROCESSOR
Data
WRITE
MODULE
READ
MODULE
To communications
channel
320
340
302

FIG. 3

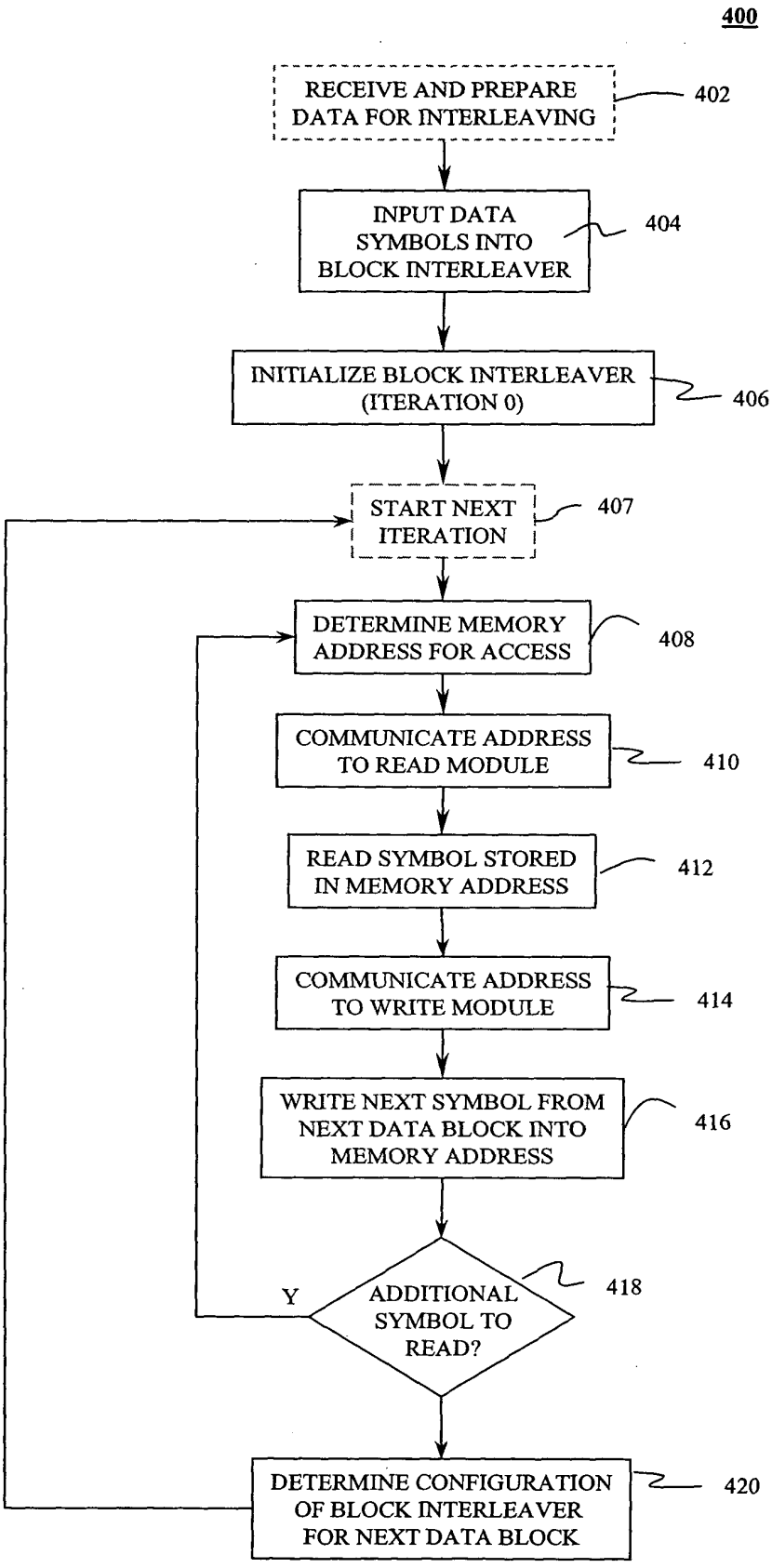
400
RECEIVE AND PREPARE DATA FOR INTERLEAVING
402
INPUT DATA SYMBOLS INTO BLOCK INTERLEAVER
404
INITIALIZE BLOCK INTERLEAVER (ITERATION 0)
406
START NEXT ITERATION
407
DETERMINE MEMORY ADDRESS FOR ACCESS
408
COMMUNICATE ADDRESS TO READ MODULE
410
READ SYMBOL STORED IN MEMORY ADDRESS
412
COMMUNICATE ADDRESS TO WRITE MODULE
414
WRITE NEXT SYMBOL FROM NEXT DATA BLOCK INTO MEMORY ADDRESS
416
ADDITIONAL SYMBOL TO READ?
418
Y
DETERMINE CONFIGURATION OF BLOCK INTERLEAVER FOR NEXT DATA BLOCK
420

FIG. 4

A_0	A_1	A_2	0
A_3	A_4	A_5	0
0	0	0	0

FIG. 5

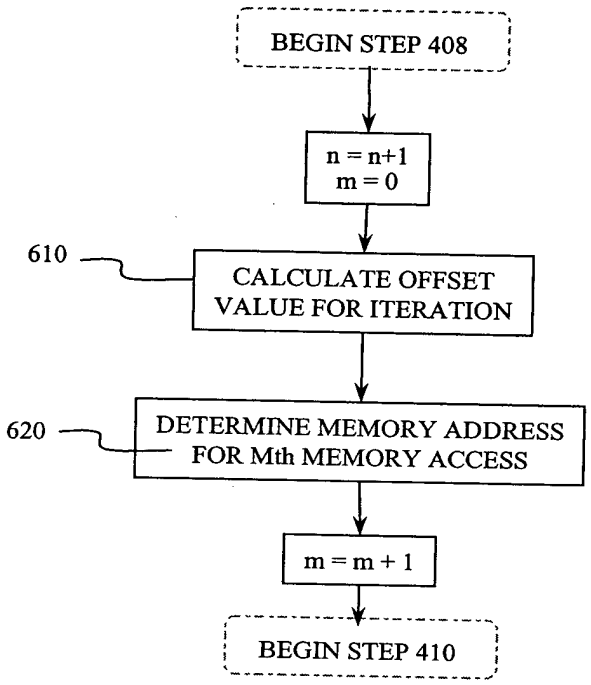
600
BEGIN STEP 408
n = n+1
m = 0
610
CALCULATE OFFSET VALUE FOR ITERATION
620
DETERMINE MEMORY ADDRESS FOR Mth MEMORY ACCESS
m = m + 1
BEGIN STEP 410

FIG. 6A

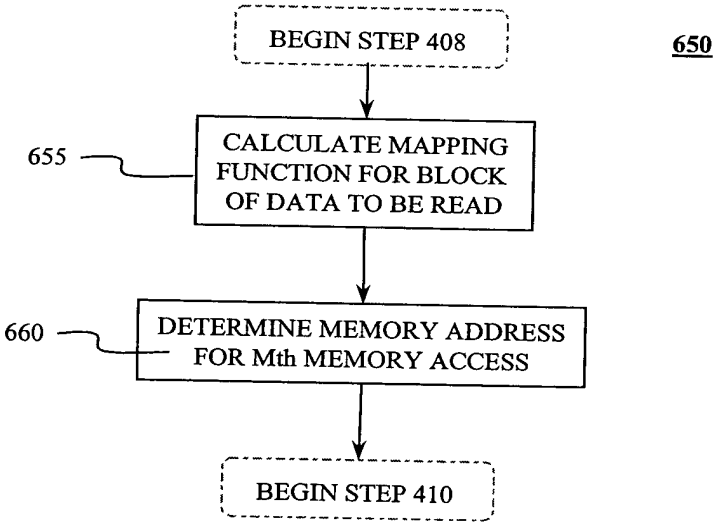
650
BEGIN STEP 408
655
CALCULATE MAPPING FUNCTION FOR BLOCK OF DATA TO BE READ
660
DETERMINE MEMORY ADDRESS FOR Mth MEMORY ACCESS
BEGIN STEP 410

FIG. 6B

730

0 A_0	1 A_1	2 A_2	3 A_3
4 A_4	5 A_5	6 A_6	7 A_7
8 A_8	9 A_9	10 A_{10}	11 A_{11}

FIG. 7A

730

0 B_0	1 B_3	2 B_6	3 B_9
4 B_1	5 B_4	6 B_7	7 B_{10}
8 B_2	9 B_5	10 B_8	11 B_{11}

FIG. 7B

730

0 C_0	1 C_9	2 C_7	3 C_5
4 C_3	5 C_1	6 C_{10}	7 C_8
8 C_6	9 C_4	10 C_2	11 C_{11}

FIG. 7C

730

0 D_0	1 D_7	2 D_3	3 D_{10}
4 D_6	5 D_2	6 D_9	7 D_5
8 D_1	9 D_8	10 D_4	11 D_{11}

FIG. 7D

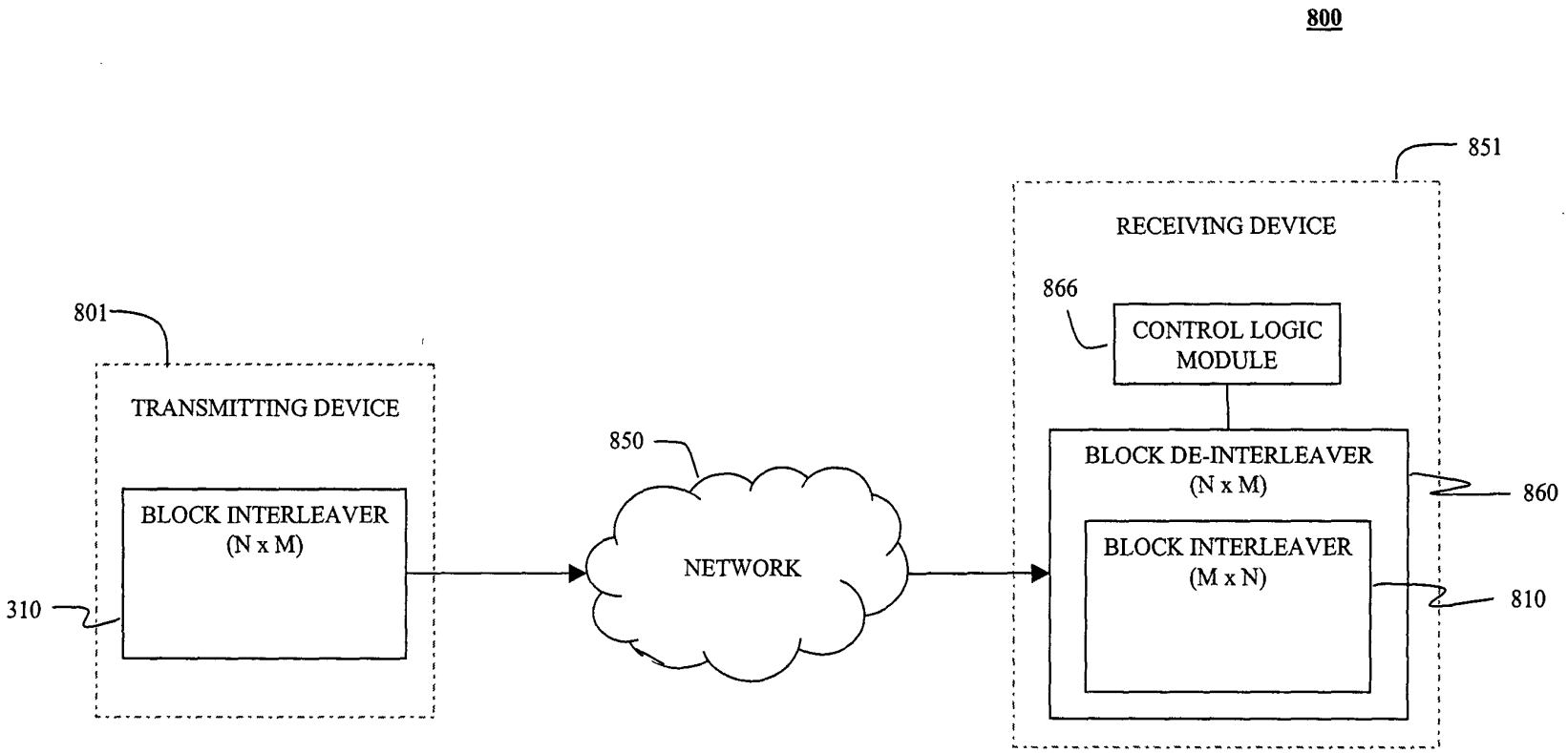
800
851
RECEIVING DEVICE
866
CONTROL LOGIC MODULE
801
TRANSMITTING DEVICE
850
BLOCK DE-INTERLEAVER (N x M)
860
BLOCK INTERLEAVER (N x M)
NETWORK
BLOCK INTERLEAVER (M x N)
310
810

FIG. 8